## EXPERIMENT - 1

## VERIFICATION OF KIRCHHOFF'S CURRENT AND VOLTAGE LAWS

## AIM:

To verify Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) in a passive resistive network

## APPARATS REQUIRED:

| S. No | Apparatus Name | Range | Type | Quantity |
| :---: | :---: | :---: | :---: | :---: |
| 1 | RPS | $(0-30) \mathrm{V}$ | Digital | 01 |
| 2 | Ammeter | $(0-200) \mathrm{mA}$ | Digital | 03 |
| 3 | Voltmeter | $(0-30) \mathrm{V}$ | Digital | 03 |
| 4 | Resistors | $330 \Omega, 100 \Omega, 330$ <br> $\Omega$ | - | 01 |
| 5 | Bread Board | - | WB102 | 01 |
| 6 | Connecting Wires | - | Single strand | Required |

## PROCEDURE:

TO VERIFY KVL

1. Connect the circuit diagram as shown in Figure.
2. Switch ON the supply to RPS.
3. Apply the voltage (say 5 v ) and note the voltmeter readings.
4. Sum up the voltmeter readings (voltage drops), that should be equal to applied voltage.
5. Thus KVL is verified practically.

## TO VERIFY KCL

1. Connect the circuit diagram as shown in Figure.
2. Switch ON the supply to RPS.
3. Apply the voltage (say 5 v ) and note the ammeter readings.
4. Sum up the Ammeter readings (I1 and I2), that should be equal to total current (I).
5. Thus KCL is verified practically.

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Make sure of proper color coding of resistors.
3. The terminal of the resistance should be properly connected.

## RESULT:

| At 15V supply | Theoretical value | Practical value |
| :---: | :---: | :---: |
| $\mathbf{V}_{\mathbf{1}}+\mathbf{V}_{\mathbf{2}}+\mathbf{V}_{\mathbf{3}}$ |  |  |
| $\mathbf{I}_{\mathbf{1}}+\mathbf{I}_{\mathbf{2}}$ |  |  |

## TABULAR COLUMN:

FOR KVL

| Applied <br> Voltage <br> V (volts) | $\mathbf{V}_{\mathbf{1}}$ (volts) |  |  | $\mathbf{V}_{\mathbf{2}}$ (volts) |  | $\mathbf{V}_{\mathbf{3}}$ (volts) |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathbf{V}_{\mathbf{1}}+\mathbf{V}_{\mathbf{2}}+\mathbf{V}_{\mathbf{3}}$ (volts) |  |  |  |  |  |
|  | Theoretical | Practical | Theoretical | practical | Theoretical | practical | Theoretical | practical |
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## FOR KCL

| Applied <br> Voltage <br> V (volts) | I (A) |  | $\mathrm{I}_{1}(\mathrm{~A})$ |  | $\mathrm{I}_{2}(\mathrm{~A})$ |  | $\mathrm{I}_{1}+\mathrm{I}_{\mathbf{2}}(\mathrm{A})$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Theoretical | Practical | Theoretical | practical | Theoretical | practical | Theoretical | practical |

CIRCUIT DIAGRAM:
TO VERIFY KVI.


CIRCUIT DIAGRAM:
TO VERIFY KVI.


## EXPERIMENT - 2

## VERIFICATION OF MAXIMUM POWER TRANSFER THEOREM

AIM: To verify Maximum Power Transfer Theorem for given circuit.

## APPARATUS REQUIRED:

| S.No. | Apparatus Name | Range | Quantity |
| :---: | :---: | :---: | :---: |
| 1 |  <br> connecting wires | - | Required |
| 2 | Resistors | $1.2 \mathrm{~K} \Omega$ | 1 |
| 3 | Ammeter | $(0-200) \mathrm{mA}$ | 1 |
| 4 | Voltmeter | $(0-30) \mathrm{V}$ | 1 |
| 5 | RPS | $(0-30) \mathrm{V}$ | 1 |
| 6 | DRB | - | 1 |

THEORY: In a linear bilateral circuit, the maximum power will be transferred from a source to a load when the load resistance is equal to the source resistance.

## PROCEDURE:

1. Connections are given as per the diagram and set a particular voltage in RPS.
2. Vary RL and note down the corresponding ammeter and Voltmeter Reading.
3. Repeat the procedure for different values of RL and Tabulate it,
4. Calculate the power for each value of RL.

## PRECAUTIONS:

1. Voltage control knob of RPS should be kept at minimum position
2. Current control knob of RPS should be kept at maximum position.

## RESULT :

## CIRCUIT DIAGRAM:



## MODEL GRAPH:



TABULAR COLUMN:

| S.no | $\mathrm{R}_{\mathrm{L}}(\Omega)$ | $\mathrm{V}_{\mathrm{L}}(\mathrm{V})$ | $\mathrm{I}_{\mathrm{L}}(\mathrm{mA})$ | $\mathrm{P}=\mathrm{V}_{\mathrm{L}} \mathrm{I}_{\mathrm{L}}(\mathrm{W})$ |
| :--- | :--- | :--- | :--- | :--- |
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## EXPERIMENT-3

## DETERMINATION OF PHASE ANGLE FOR RC SERIES CIRCUIT

AIM: To determine the phase angle of RCSeries Circuit
APPARATUS :

| S.No | Apparatus Name | Range | Quantity |
| :---: | :---: | :---: | :---: |
| 1 | Function Generator | $10 \mathrm{~Hz}-10 \mathrm{MHz}$ | 1 |
| 2 | Resistor | $10 \mathrm{k} \Omega$ | 1 |
| 3 | Capacitor | $0.01 \mu \mathrm{~F}$ | 1 |
| 4 | CRO | - | 1 |
| 5 | Breadboard, <br> Connecting wires, <br> CRO probes | - | Required |

## PROCEDURE:

1. Connect the circuit diagram as shown
2. Switch ON the function generator and apply the sinusoidal input waveform at 1 KHz frequency.
3. Connect CRO probe at function generator terminals and check input at channel 1.
4. Connect CRO probe between R and C terminals and observe the output in channel 2 .
5. Calculate the phase angle between input and output

## PRECAUTIONS :

1. Check for proper connections before switching the supply ON
2. Make sure of proper color coding of resistor
3. Avoid parallax error in measuring instrument.

RESULT:

## CIRCUIT DIAGRAM:



## MODEL GRAPGH:



TABULAR COLOUMN

| S.No | INPUT |  | OUTPUT |  |
| :--- | :---: | :---: | :---: | :---: |
|  | Time Period <br> $(\mathrm{T} \mathrm{sec})$ | Angle ( $\theta$ ) | Time Period <br> (T sec) | Angle ( $\theta$ ) |
|  |  |  |  |  |
|  |  |  |  |  |

## EXPERIMENT-4

## BRAKE TEST ON DC SHUNT MOTOR

AIM: To obtain the performance characteristics of DC shunt motor by direct loading.
APPARATUS REQUIRED:

| S. No. | Name of the Equipment | Range | Type | Quantity |
| :--- | :--- | :--- | :--- | :--- |
| 1. | Voltmeter | $0-300 \mathrm{~V}$ | M.C | 01 |
| 2. | Ammeter | $0-2 \mathrm{~A}$ | M.C | 01 |
| 3. | Rheostat | Tachometer | - | - |
| 4. | Connecting wires | - | Digital | 01 |
| 5. |  |  |  | per |

## PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Keeping the field rheostat $\left(\mathrm{R}_{\mathrm{f}}\right)$ at the minimum position, switch on the supply and start the motor.
3. Adjust the speed of the motor on no load to its rated value by means of the field rheostat. Do not distrub the position of the rheostat through out the test.
4. Put on the load by tightening the screws of the spring balances. Note down the spring tensions, the speed, the voltage and the currents at different loads until full load current obtained.

## PRECAUTIONS:

(i) Connections must be made tight
(ii) Before making or breaking the circuit, supply must be switched off

## RESULT:

## CIRCUIT DIAGRAM:



TABULAR COLUMN:
Radius of Brake Drum: 0.16 m


Radius of Brake Drum:

## MODEL GRAPHS:




## THEORETICAL CALCULATIONS:

1. Measure the circumference of the brake drum and calculate its radius ( r ), in meters.
2. Calculate the torque, $T=\operatorname{Srg}(N . m)$. Where $S=S_{1}-S_{2}=$ spring balance reading (the difference between the spring tensions) and ' g ' is acceleration due to gravity i.e.9.81. Calculate the power output of the motor given by $\mathrm{P}_{0}=2 \Pi \mathrm{NT} / 60$
3. Calculate the input power, $\mathrm{P}_{\mathrm{I}}=\mathrm{VI}_{\mathrm{L}}\left(\mathrm{I}_{\mathrm{L}}\right.$ is the line current $=\left(\mathrm{I}_{\mathrm{a}}+\mathrm{I}_{\mathrm{f}}\right)$.
4. Calculate the percentage efficiency, $\eta=\mathrm{P}_{0} / \mathrm{P}_{\mathrm{I}} 100$

CIRCUIT DIAGRAM:
LOAD TEST ON IPH TRANSFORMER


## FUSERATING:

$125 \%$ of rated current

NAME PLATE DETAILS:
Primary
Secondary

Rated Woltage Rated Current Rated Porer

## EXPERIMENT-5

## LOAD TEST ON A SINGLE PHASE TRANSFORMER

AIM: To find the efficiency and regulation of single phase transformer by using load test.

## APPARATUS REQUIRED:

| S.No. | Apparatus | Range | Type | Quantity |
| :---: | :--- | :---: | :---: | :---: |
| 1 | Ammeter | $(0-10) \mathrm{A}$ | MI | 1 |
| 2 | Voltmeter | $(0-5) \mathrm{A}$ | MI | 1 |
| 3 | Wattmeter | $(0-150) \mathrm{V}$ | MI | 1 |
|  |  | $(300 \mathrm{~V}, 5 \mathrm{~A})$ | UPF | 1 |
| 4 | Auto Transformer | $1 \phi,(0-260) \mathrm{V}$ | - | 1 |
| 5 | Resistive Load | $5 \mathrm{KW}, 230 \mathrm{~V}$ | - | 1 |
| 6 | Connecting Wires | $2.5 \mathrm{sq} . \mathrm{mm}$ | Copper | as per |
|  |  |  |  |  |

TABULAR COLUMN:

| S.No. | Load | Primary |  |  | Secondary |  |  | Input <br> Power $\mathbf{W}_{1} \times \mathbf{M F}$ | Output Power$\mathbf{W}_{2} \times \mathbf{M F}$ | Efficiency <br> $\eta$ $\%$ | Regulation |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $V_{1}$ <br> (Volts) | $\mathrm{I}_{1}$ (Amps) | $\mathrm{W}_{1}$ <br> (Watts) | $V_{2}$ <br> (Volts) | $\begin{gathered} \mathrm{I}_{2} \\ (\mathrm{Amps}) \end{gathered}$ | $\mathbf{W}_{2}$ <br> (Watts) |  |  |  |  |

## PROCEDURE:

1. Connections are made as per the circuit diagram.
2. After checking the no load condition, minimum position of auto transformer and DPST switch is closed.
3. Ammeter, Voltmeter and Wattmeter readings on both primary side and secondary side are noted.
4. The load is increased and for each load, Voltmeter, Ammeter and Wattmeter readings on both primary and secondary sides are noted.
5. Again no load condition is obtained and DPST switch is opened.

## PRECAUTIONS:

1. Auto Transformer should be in minimum position.
2. The AC supply is given and removed from the transformer under no load condition

## RESULT:

Thus we have been obtained the characteristic curve of $1 \varphi$ transformer

## THEORETICAL CALCULATIONS:

Output Power $=\mathrm{W}_{2} \times$ Multiplication factor
Input Power $=\mathrm{W}_{1} \times$ Multiplication factor

Efficiency $\eta \%=\frac{\text { Output power }}{\text { Input } \text { power }} \times 100 \%$
$\mathrm{V}_{\mathrm{NL}}-\mathrm{V}_{\mathrm{FL}}$ (Secondary)
Regulation R \% = ----------------------------- x $100 \%$
$V_{N L}$

## EXPERIMENT-6 <br> BRAKE TEST ON 3- $\Phi$ SQUIRREL CAGE INDUCTION MOTOR

AIM:
To determine the efficiency of 3- $\phi$ induction motor by performing load test. To obtain the performance curves for the same.

## APPARATUS REQUIRED:

| Sl. | Equipment | Type | Range | Quantity |
| :--- | :--- | :--- | :--- | :--- |
| 1 | Voltmeter | MI | $(0-600) \mathrm{V}$ | 1 no |
| 3 | Ammeter | MI | $(0-10) \mathrm{A}$ | 1 no |
| 2 | Wattmeter | Electro dynamo meter type | $10 \mathrm{~A} / 600 \mathrm{~V}$ UPF | 1 no |
| 4 | Tachometer | Digital | $10 \mathrm{~A} / 600 \mathrm{~V}$ LPF | 1 no |
| 5 | Connecting Wires | ------ |  | Required |

## CIRCUIT DIAGRAM:



## MODEL GRAPHS:

1. Speed or slip Vs output power
2. Torque Vs output power
3. \% efficiency Vs output power





## PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Ensure that the $3-\phi$ variac is kept at minimum output voltage position and belt is freely suspended.
3. Switch ON the supply. Increase the variac output voltage gradually until rated voltage is observed in voltmeter. Note that the induction motor takes large current initially, so, keep an eye on the ammeter such that the starting current current should not exceed 7 Amp.
4. By the time speed gains rated value, note down the readings of voltmeter, ammeter, and wattmeter at no-load.
5. Now the increase the mechanical load by tightening the belt around the brake drum gradually in steps.
6. Note down the various meters readings at different values of load till the ammeter shows the rated current.
7. Reduce the load on the motor finally, and switch OFF the supply.

## PRECAUTIONS:

1. Connections must be made tight
2. Before making or breaking the circuit, supply must be switched off

## RESULT:

## EXPERIMENT-7 <br> V-I CHARACTERISTICS OF PN JUNCTION DIODE

## AIM:

To study the PN junction diode characteristics under Forward \& Reverse bias conditions.

APPARATUS REQUIRED

| S.No. | Name | Range | Qty |
| :---: | :--- | :---: | :---: |
| 1 | R.P.S | $(0-30) \mathrm{V}$ | 1 |
| 2 | Ammeter | $(0-200) \mu \mathrm{A}$ | 1 |
| 3 | Voltmeter | $(0-20) \mathrm{V}$ | 1 |

COMPONENTS REQUIRED

| S.No. | Name | Range | Qty |
| :---: | :--- | :---: | :---: |
| 1 | Diode | IN4007 | 1 |
| 2 | Resistor | $1 \mathrm{k} \boldsymbol{\Omega}$ | 1 |
| 3 | Connecting <br> Wires | - | set |

## THEORY:

A PN junction diode is a two terminal junction device. It conducts only in one direction (only on forward biasing).

## FORWARD BIAS:

On forward biasing, initially no current flows due to barrier potential. As the applied potential exceeds the barrier potential the charge carriers gain sufficient energy to cross the potential barrier and hence enter the other region. The holes, which are majority carriers in the P-region, become minority carriers on entering the N -regions, and electrons, which are the majority carriers in the N-region, become minority carriers on entering the P-region. This injection of Minority carriers results in the current flow, opposite to the direction of electron movement.

## REVERSE BIAS:

On reverse biasing, the majority charge carriers are attracted towards the terminals due to the applied potential resulting in the widening of the depletion region. Since the charge carriers are pushed towards the terminals no current flows in the device due to majority charge carriers. There will be some current in the device due to the thermally generated minority carriers. The generation of such carriers is independent of the applied potential and hence the current is constant for all increasing reverse potential.

This current is referred to as Reverse Saturation Current ( $\mathrm{I}_{\mathrm{O}}$ ) and it increases with temperature. When the applied reverse voltage is increased beyond the certain limit, it results in breakdown. During breakdown, the diode current increases tremendously.

## PROCEDURE:

## FORWARD BIAS:

1. Connect the circuit as per the diagram.
2. Vary the applied voltage V in steps of 0.1 V .
3. Note down the corresponding Ammeter readings $\mathrm{I}_{\mathrm{f}}$.
4. Plot a graph between $\mathrm{V}_{\mathrm{f}} \& \mathrm{I}_{\mathrm{f}}$

## REVERSE BIAS:

1. Connect the circuit as per the diagram.
2. Vary the applied voltage $\mathrm{V}_{\mathrm{r}}$ in steps of 0.1 V .
3. Note down the corresponding Ammeter readings $I_{r}$.
4. Plot a graph between $\mathbf{V}_{\mathbf{r}} \& \mathbf{I}_{\mathbf{r}}$

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Make sure of proper color coding of resistors.
3. The terminal of the resistance should be properly connected.

## RESULT:

Forward and Reverse bias characteristics of the PN junction diode was Studied

## CIRCUIT DIAGRAM:

## FORWARD BIAS:



## REVERSE BIAS:



## MODEL GRAPH



## TABULAR COLUMN:

FORWARD BIAS:
REVERSE BIAS:


## EXPERIMENT-8

## V- I CHARACTERISTICS OF ZENER DIODE

AIM: To study the V-I characteristics and to determine the breakdown voltage of a zener diode.

APPARATUS REQUIRED

| S.No. | Name | Range | Qty |
| :---: | :---: | :---: | :---: |
| 1 | R.P.S | $(0-30) \mathrm{V}$ | 1 |
| 2 | Ammeter | $(0-20) \mathrm{mA}$ | 1 |
| 3 | Voltmeter | $(0-30) \mathrm{V}$ | 1 |

COMPONENTS REQUIRED

| S.No | Name | Range | Qty |
| :---: | :---: | :---: | :---: |
| 1 | zener diode | 3.9 V | 1 |
| 2 | Resistor | $1 \mathrm{~K} \Omega$ | 1 |
| 3 | Breadboard | - | 1 |
| 4 | Wires | - |  |

## THEORY:

A properly doped crystal diode, which has a sharp breakdown voltage, is known as zener diode.

## FORWARD BIAS:

On forward biasing, initially no current flows due to barrier potential. As the applied potential increases, it exceeds the barrier potential at one value and the charge carriers gain sufficient energy to cross the potential barrier and enter the other region. the holes, which are majority carriers in p-region, become minority carriers on entering the N -regions and electrons, which are the majority carriers in the N -regions become minority carriers on entering the P-region. This injection of minority carriers results current, opposite to the direction of electron movement.

## REVERSE BIAS:

When the reverse bias is applied due to majority carriers small amount of current (ie) reverse saturation current flows across the junction. As the reverse bias is increased to breakdown voltage, sudden rise in current takes place due to zener effect.

## ZENER EFFECT:

Normally, PN junction of Zener Diode is heavily doped. Due to heavy doping the depletion layer will be narrow. When the reverse bias is increased the potential across the depletion layer is more. This exerts a force on the electrons in the outermost shell. Because of this force the electrons are pulled away from the parent nuclei and become free electrons. This ionization, which occurs due to electrostatic force of attraction, is known as Zener effect. It results in large number of free carriers, which in turn increases the reverse saturation current

## PROCEDURE:

## REVERSE BIAS:

1. Connect the circuit as per the diagram.
2. Vary the power supply in such a way that the readings are taken in steps of 0.5 V .
3. Note down the corresponding Ammeter readings $\mathbf{I}_{\mathbf{r}}$.
4. Plot a graph between $\mathbf{V}_{\mathbf{r}} \boldsymbol{\&} \mathbf{I}_{\mathbf{r}}$

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Make sure of proper color coding of resistors.
3. The terminal of the resistance should be properly connected.

## RESULT:

Forward and Reverse bias characteristics of the zener diode was studied

## CIRCUIT DIAGRAM:

## REVERSE BIAS:



## MODEL GRAPH:



## REVERSE BIAS:

| S.No. | VOLTAGE ( $\mathbf{V}_{\mathrm{r}}$ ) <br> ( V$)$ | $\begin{gathered} \text { CURRENT }\left(\mathrm{I}_{\mathrm{r}}\right) \\ (\mathrm{mA}) \end{gathered}$ |
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## EXPERIMENT - 9

## HALF WAVE RECTIFIER \& FULLWAVE WAVE RECTIFIER

AIM: To Rectify the signal and then to find Ripple Factor, Efficiency and Percentage of Regulation in Full Wave and Half Wave Rectifier without filters.

## APPARATUS:

| S.No | Name of the equipment | Range | Quantity |
| :--- | :--- | :--- | :--- |
| 1 | Transformer | $230 \mathrm{v} / 6 \mathrm{v}-0-6 \mathrm{v}$ | 1 |
| 2 | PN Junction Diode | IN 4007 | 3 |
| 3 | Resistance | $10 \mathrm{~K} \Omega$ | 2 |
| 4 | Multimeter | - | 1 |
| 5 | 20MHz Dual Trace CRO | - | 1 |
| 6 | Bread Board, Connecting <br> Wires | - | Required |

## PROCEDURE:

1. Connecting the circuit on breadboard as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e $230 \mathrm{v}, 50 \mathrm{~Hz}$.
3. Connect the decade resistance box and set the $R_{L}$ value to $500 \Omega$.
4. Connect the multimeter at output terminals and vary the load resistance (DRB) from $500 \Omega$ to $5 \mathrm{k} \Omega$ and note down the Vac and Vdc as per given tabular form.
5. Disconnect load resistance (DRB) and note down no load voltage Vdc.
6. Connect load resistance at $5 \mathrm{~K} \Omega$ and connect channel-II of CRo at output terminals and $\mathrm{CH}-\mathrm{I}$ of CRO at Secondary Input terminals observe and note down the Input and Output Waveform on Graph Sheet

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Avoid loose connections.
3. The terminal of the diode should be properly connected.

## RESULT:

Observe input and output waveforms of halfwave and fullwave rectifiers.

## CIRCUIT DIAGRAM:

## HALFWAVE RECTIFIER



## FULL WAVE RECTIFIER



## MODEL GRAPH:



FULL WAVE WITHOUT FILTER


HALF WAVE WITHOUT FILTER

## EXPERIMENT-10 <br> INPUT \& OUTPUT CHARACTERISTICS OF TRANSISTOR IN CE CONFIGURATION

AIM: To study and plot the transistor characteristics in CE configuration.
APPARATUS REQUIRED:

| S.No. | Name | Range | Qty |
| :---: | :--- | :--- | :---: |
| 1 | R.P.S | $(0-30) \mathrm{V}$ | 2 |
| 2 | Ammeter | $(0-20) \mathrm{mA}$ | 1 |
|  |  | $(0-200) \mu \mathrm{A}$ | 1 |
| 3 | Voltmeter | $(0-20) \mathrm{V}$ | 2 |

COMPONENTS REQUIRED:

| S.No. | Name | Range | Qty |
| :---: | :--- | :--- | :---: |
| 1 | Transistor | BC 107 | 1 |
| 2 | Resistor | $1 \mathrm{~K} \Omega$ | 1 |
| 3 | Bread |  | 1 |
| 4 | Wires |  |  |

## THEORY:

A BJT is a three terminal two - junction semiconductor device in which the conduction is due to both the charge carrier. Hence it is a bipolar device and it amplifier the sine waveform as they are transferred from input to output. BJT is classified into two types - NPN or PNP. A NPN transistor consists of two N types in between which a layer of P is sandwiched. The transistor consists of three terminal emitter, collector and base. The emitter layer is the source of the charge carriers and it is heartily doped with a moderate cross sectional area. The collector collects the charge carries and hence moderate doping and large cross sectional area. The base region acts a path for the movement of the
charge carriers. In order to reduce the recombination of holes and electrons the base region is lightly doped and is of hollow cross sectional area. Normally the transistor operates with the EB junction forward biased.

In transistor, the current is same in both junctions, which indicates that there is a transfer of resistance between the two junctions. Hence known as transfer resistance of transistor.

## PROCEDURE:

## INPUT CHARECTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set $\mathrm{V}_{\mathrm{CE}}$, vary $\mathrm{V}_{\mathrm{BE}}$ in regular interval of steps and note down the corresponding $\mathrm{I}_{\mathrm{B}}$ reading. Repeat the above procedure for different values of $\mathrm{V}_{\mathrm{CE}}$.
3. Plot the graph: $\mathrm{V}_{\mathrm{BE}} \mathrm{Vs}_{\mathrm{I}}$ for a constant $\mathrm{V}_{\mathrm{CE}}$.

## OUTPUT CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set $\mathrm{I}_{\mathrm{B}}$, Vary $\mathrm{V}_{\mathrm{CE}}$ in regular interval of steps and note down the corresponding $\mathrm{I}_{\mathrm{C}}$ reading. Repeat the above procedure for different values of $\mathrm{I}_{\mathrm{B}}$.
3. Plot the graph: $\mathrm{V}_{\mathrm{CE}}$ Vs $\mathrm{I}_{\mathrm{C}}$ for a constant $\mathrm{I}_{\mathrm{B}}$.

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Avoid loose connections.
3. The terminal of the BJT should be properly connected.

## RESULT:

The transistor characteristics of a Common Emitter (CE) configuration were plotted.

## PIN DIAGRAM:

B

Bottom View BC107

E


## CIRCUIT DIAGRAM:



MODEL GRAPH:

INPUT CHARACTERISTICS:


OUTPUT CHARACTERISTICS:


TABULAR COLUMN:
INPUT CHARACTERISTICS:

| $\mathrm{V}_{\mathrm{CE}}=\mathrm{V}$ |  |  |  |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{BE}}(\mathrm{V})$ | $\mathrm{I}_{\mathrm{B}}(\mu \mathrm{A})$ | $\mathrm{V}_{\mathrm{BE}}(\mathrm{V})$ | $\mathrm{V}_{\mathrm{CE}}=\mathrm{V}$ |
|  |  |  | $\mathrm{I}_{\mathrm{B}}(\mu \mathrm{H})$ |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

OUTPUT CHARACTERISTICS:

| $I_{B}=\mu A$ |  |  | $I_{B}=\mu A$ |
| :---: | :---: | :---: | :---: |
|  | $\mathrm{~V}_{\mathbf{C E}}(\mathrm{V})$ |  | $I_{C}(\mathrm{~mA})$ |
|  |  | $\mathrm{V}_{\mathrm{CE}}(\mathrm{V})$ |  |
|  |  |  |  |

## EXPERIMENT-11

## INPUT \& OUTPUT CHARACTERISTICS OF BJT WITH CB CONFIGURATION

AIM: To study and plot the transistor characteristics in CB configuration.

APPARATUS REQUIRED:

| S.No. | Name | Range | Qty |
| :---: | :--- | :--- | :---: |
| 1 | R.P.S | $(0-30) \mathrm{V}$ | 2 |
| 2 | Ammeter |  |  |
| 3 | Voltmeter | $(0-20) \mathrm{mA}$ | 2 |
|  |  |  |  |

COMPONENTS REQUIRED:

| S.No. | Name | Range | Qty |
| :---: | :--- | :--- | :---: |
| 1 | Transistor | BC 107 | 1 |
| 2 | Resistor | $1 \mathrm{~K} \Omega$ | 1 |
| 3 | Bread <br> Board | ---- | 1 |
| 4 | Wires |  | AS PER <br> Reuired |

## THEORY:

In this configuration the base is made common to both the input and out. The emitter is given the input and the output is taken across the collector. The current gain of this configuration is less than unity. The voltage gain of CB configuration is high. Due to the high voltage gain, the power gain is also high. In CB configuration, Base is common to both input and output. In CB configuration the input characteristics relate $I_{E}$ and $V_{E B}$ for a constant $V_{C B}$. Initially let $V_{C B}=0$ then the input junction is equivalent to a forward biased diode and the characteristics resembles that of a diode. Where $V_{C B}=+V_{I}$ (volts) due to early effect $\mathrm{I}_{\mathrm{E}}$ increases and so the characteristics shifts to the left. The output characteristics relate $\mathrm{I}_{\mathrm{C}}$ and $\mathrm{V}_{\mathrm{CB}}$ for a constant $\mathrm{I}_{\mathrm{E}}$. Initially $\mathrm{I}_{\mathrm{C}}$ increases and then it levels for a value $\mathrm{I}_{\mathrm{C}}=\alpha \mathrm{I}_{\mathrm{E}}$. When $\mathrm{I}_{\mathrm{E}}$ is increased $\mathrm{I}_{\mathrm{C}}$ also increases proportionality. Though increase in $\mathrm{V}_{\mathrm{CB}}$ causes an increase in $\alpha$, since $\alpha$ is a fraction, it is negligible and so $I_{C}$ remains a constant for all values of $\mathrm{V}_{\mathrm{CB}}$ once it levels off.

## PROCEDURE:

## INPUT CHARACTERISTICS:

1. It is the curve between emitter current $\mathrm{I}_{\mathrm{E}}$ and emitter-base voltage $\mathrm{V}_{\mathrm{BE}}$ at constant collector-base voltage $\mathrm{V}_{\mathrm{CB}}$.
2. Connect the circuit as per the circuit diagram.
3. Set $\mathrm{V}_{\mathrm{CB}}$, vary $\mathrm{V}_{\mathrm{BE}}$ in steps and note down the corresponding $\mathrm{I}_{\mathrm{E}}$
4. Plot the graph $\mathrm{V}_{\mathrm{BE}} \mathrm{Vs} \mathrm{I}_{\mathrm{E}}$ for a constant $\mathrm{V}_{\mathrm{CB}}$.

## OUTPUT CHARACTERISTICS:

1. It is the curve between collector current $\mathrm{I}_{\mathrm{C}}$ and collector-base voltage $\mathrm{V}_{\mathrm{CB}}$ at constant emitter current $\mathrm{I}_{\mathrm{E}}$.
2. Connect the circuit as per the circuit diagram.
3. Set $\mathrm{I}_{\mathrm{E}}$, vary $\mathrm{V}_{\mathrm{CB}}$ in steps and note down the corresponding $\mathrm{I}_{\mathrm{C}}$.
4. Plot the graph $\mathrm{V}_{\mathrm{CB}}$ Vs $\mathrm{I}_{\mathrm{C}}$ for a constant $\mathrm{I}_{\mathrm{E}}$.

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Avoid loose connections.
3. The terminal of the BJT should be properly connected.

## RESULT:

The transistor characteristics of a Common Base (CB) configuration were plotted and studied

## CIRCUIT DIAGRAM:

$$
(0-20) \mathrm{mA} \quad(0-20) \mathrm{mA}
$$



TABULAR COLUMN:
INPUT CHARACTERISTICS:

| S.No. | $\mathrm{V}_{\mathrm{CB}}=\quad \mathrm{V}$ |  | $\mathrm{V}_{\mathrm{CB}}=\quad \mathrm{V}$ |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $V_{\text {eb }}$ <br> (V) | $\begin{gathered} \mathrm{I}_{\mathrm{E}} \\ (\mathrm{~mA}) \end{gathered}$ | $V_{\text {Eb }}$ <br> (V) | $\begin{gathered} \mathrm{I}_{\mathrm{E}} \\ (\mathrm{~mA}) \end{gathered}$ |
|  |  |  |  |  |

OUTPUT CHARACTERISTICS:

| S.No. | $\mathrm{I}_{\mathrm{E}}=$ | mA | $\mathrm{I}_{\mathrm{E}}=$ | mA |
| :---: | :---: | :---: | :---: | :---: |
|  | Vcb <br> (V) | $\begin{gathered} \text { Ic } \\ \text { (mA) } \end{gathered}$ | Vcb <br> (V) | $\begin{gathered} \text { Ic } \\ (\mathrm{mA}) \end{gathered}$ |
|  |  |  |  |  |

## MODEL GRAPH:

## INPUT CHARACTERISTICS:



## OUTPUT CHARACTERISTICS:



## EXPERIMENT-12

INPUT AND OUTPUT CHARACTERISTICS OF JFET

AIM: To Plot the characteristics of JFET

APPARATUS REQUIRED:

| S.No. | Name | Range | Type | Qty |
| :---: | :--- | :--- | :--- | :---: |
| 1 | R.P.S | $(0-30) \mathrm{V}$ | Digital | 2 |
| 2 | Ammeter | $(0-20) \mathrm{mA}$ | Digital | 1 |
| 3 | Voltmeter |  |  |  |
|  | $(0-20) \mathrm{V}$ | Digital | 2 |  |

## COMPONENTS REQUIRED:

| S.No. | Name | Range | Type | Qty |
| :---: | :--- | :--- | :---: | :---: |
| 1 | FET | BFW10 | ----- | 1 |
| 2 | Resistor | $470 \Omega$ | ---- | 2 |
| 3 | Bread |  |  | 1 |
| 4 | Board | ----- | ---- |  |

## THEORY:

FET is a voltage operated device. It has got 3 terminals. They are Source, Drain \& Gate. When the gate is biased negative with respect to the source, the pn junctions are reverse biased \& depletion regions are formed. The channel is more lightly doped than the $p$ type gate, so the depletion regions penetrate deeply in to the channel. The result is that the channel is narrowed, its resistance is increased, \& $\mathrm{I}_{\mathrm{D}}$ is reduced. When the negative bias voltage is further increased, the depletion regions meet at the center $\& \mathrm{I}_{\mathrm{D}}$ is cutoff completely.

## PROCEDURE:

## DRAIN CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set the gate voltage $\mathrm{V}_{\mathrm{GS}}$.
3. Vary $\mathrm{V}_{\mathrm{DS}}$ in steps \& note down the corresponding $\mathrm{I}_{\mathrm{D}}$.
4. Repeat the same procedure for different values of $\mathrm{V}_{\mathrm{GS}}$.
5. Plot the graph $V_{D S}$ Vs $I_{D}$ for constant $V_{G S}$.

## TRANSFER CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set the drain voltage $\mathrm{V}_{\mathrm{DS}}$.
3. Vary the gate voltage $\mathrm{V}_{\mathrm{GS}}$ in steps \& note down the corresponding $\mathrm{I}_{\mathrm{D}}$.
4. Repeat the same procedure for different values of $V_{D S}$.
5. Plot the graph $\mathrm{V}_{\mathrm{GS}} \mathrm{Vs} \mathrm{I}_{\mathrm{D}}$ for constant $\mathrm{V}_{\mathrm{DS}}$.

## PRECAUTIONS:

1. Check for proper connections before switching ON the supply.
2. Avoid loose connections.
3. The terminal of the FET should be properly connected.

## RESULT:

Thus the Drain \& Transfer characteristics of given FET is Plotted.

## CIRCUIT DIAGRAM:



PIN DIAGRAM:

## BOTTOM VIEW OF BFW10:



## SPECIFICATION:

Voltage : 30V, IDSS $>8 \mathrm{~mA}$.

MODEL GRAPH:
DRAIN CHARACTERISTICS:


TRANSFER CHARACTERISTICS:


TABULAR COLUMN:
DRAIN CHARACTERISTICS:

| $V_{G S}=0 V$ |  |  | $V_{G S}=-1 V$ |
| :---: | :---: | :---: | :---: |
| $V_{\text {DS }}(V)$ |  | $I_{D}(\mathrm{~mA})$ | $V_{D S}(V)$ |
|  |  |  |  |
|  |  |  |  |

TRANSFER CHARACTERISTICS:

| $V_{D S}=5$ volts |  | $V_{D S}=10$ volts |  |
| :--- | :--- | :--- | :--- |
| $V_{G S}(V)$ | $I_{D}(\mathrm{~mA})$ | $V_{G S}(V)$ | $I_{D}(\mathrm{~mA})$ |
|  |  |  |  |

